REMARKS

The examiner suggested that a new title is required that is clearly indicative of the invention. Given applicants amendments to the claims, which now specify a high-k gate dielectric layer, the title is now clearly indicative of the invention.

Rejection Under 35 U.S.C. §102

The examiner rejected claims 21 and 38 under 35 U.S.C. §102(e) as being anticipated by Kim. In response, applicants amended claim 21 to specify:

(1) "forming on a substrate a high-k gate dielectric layer that comprises a material selected from the group consisting of hafnium oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, titanium oxide, tantalum oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate;" and

(2) "forming a gate electrode that comprises polysilicon on the high-k dielectric layer."

Support for these amendments appears in the specification at page 4, lines 6-12 ("When serving as the gate dielectric for the semiconductor device, dielectric layer 101 is a "high-k gate dielectric." Some of the materials that may be used to make high-k gate dielectrics include: hafnium oxide, lanthanum oxide,

zirconium oxide, zirconium silicon oxide, titanium oxide, tantalum oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate."), and at page 7, lines 1-13 ("In a preferred embodiment, the gate electrode may be formed by initially depositing polysilicon layer 103 on high-k gate dielectric layer 101 – generating the figure 1c structure . . . . additional steps that are generally used to complete the gate electrode (e.g., forming a silicide (not shown) on the upper part of etched polysilicon structure 104) may be applied . . . . a sacrificial titanium nitride layer may enable a high-k gate dielectric to be used with a polysilicon-based gate electrode."

Although Kim indicates that "gate dielectric material 214 is comprised of a high dielectric constant material," Kim does not specify any of the materials that amended claim 21 requires. Although Kim indicates that a dummy gate electrode material (e.g., silicon nitride) may be deposited on gate dielectric material 214, that a metal oxide material (e.g., RuO_2 or IrO_2) may be deposited on PMOS gate dielectric 222, and that a metal material (e.g., aluminum, molybdenum, platinum, or tantalum) may be deposited on NMOS gate dielectric 226, Kim does not specify forming a gate electrode that comprises polysilicon on a high-k gate dielectric layer, as amended claim 21 requires. Because Kim does not describe a method that includes these two process steps, Kim does not

anticipate the method of amended claim 21, or the method of its dependent claim 38.

Rejection based on obviousness-type double patenting

The examiner rejected claims 21 and 38 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-19 of U.S. Patent No. 6,617,209 B1. In response, applicants have submitted the enclosed terminal disclaimer, which disclaims the terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. §§154 to 156 and 173 of prior U. S. Patent No. 6,617,209 B1.

In view of the submission of the enclosed terminal disclaimer, applicants respectfully request the examiner to allow amended claim 21, and its dependent claim 38, to issue.

Respectfully submitted,

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